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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590	02/17/2004		EXAMINER	
Timothy N Trop Trop Pruner & Hu PC Suite 100 8554 Katy Freeway Houston, TX 77024			FAULK, DEVONA E	
			ART UNIT	PAPER NUMBER
			2644	
			DATE MAILED: 02/17/2004	3

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/577,399	SHI ET AL.	
	Examiner	Art Unit	
	Devona E. Faulk	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 22 May 2000.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-22 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 22 May 2000 is/are: a) accepted or b) objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

    1. Certified copies of the priority documents have been received.

    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) The translation of the foreign language provisional application has been received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.

4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1,3,4,5,6, 8,10,11-17, 18,20,21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation (Audio Codec '97).

Regarding **claim 1**, Intel's document, Audio Codec '97, explaining the features, operation etc. comprises a block diagram of the functional blocks that make up the Audio Codec '97 (Figure 1)comprising a pair of D/A converters (DACs) which support a stereo PCM out channel which reads on “ a first pair of digital to analog converters coupled to one of said stereo channel pairs”; a digital interface ; a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer, which read on “a pair of analog to digital converters coupled to another one of said stereo channel pairs, one of said mixers also couple to said pair of analog to digital converters”; an analog mixer. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo

channel pair. Although Intel does not teach of a second pair of D/A converters coupled to another one of said stereo channel pairs, and another mixer to output the other audio program it would have been obvious under duplication of parts, *In Re Harza*, 274 F. 2d 669, 124, USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing the second stereo channel separately.

**Claim 3** claims the codec of claim 1 wherein said digital interface includes a plurality of programmable ports so that the connections from the digital interface to said digital-to-analog converters may be changed. As stated above apropos of claim 1, Intel meets all elements of that claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to ensure that the digital interface would have a plurality of programmable ports for the benefit of being able to process different types of audio sources.

**Claim 4** claims the codec of claim 1 wherein said digital interface has a programmably changeable output data rate. As stated above apropos of claim 1, Intel's Audio Codec '97 meets all elements of that claim. Intel discloses on page 14, paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. It would have been obvious to one of ordinary skill in the art to modify Intel's codec so that the digital interface can have a changeable output data rate for the benefit of mixing data.

3. Regarding **claim 5**, Intel's document, Audio Codec '97, explaining the features, operation etc. comprises a block diagram of the functional blocks that make up the Audio Codec '97 (Figure 1), which reads on "a processor", comprising a pair of D/A converters (DACs) which support a stereo PCM out channel which reads on "a first pair of digital to analog

converters coupled to one of said stereo channel pairs"; a digital interface ; and an analog mixer. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo channel pair. Intel further teaches of a multi-functional PCI accelerator , Figure 2; page 14, 2<sup>nd</sup> paragraph, in which the AC '97 controller would be embedded and which would be coupled to the codec. This reads on "an audio accelerator coupled to said processor". A PCI accelerator support s audio data. Although Intel does not teach of a second pair of D/A converters coupled to another one of said stereo channel pairs, and another mixer to output the other audio program it would have been obvious under duplication of parts , *In Re Harza*, 274 F. 2d 669, 124, USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing the second stereo channel separately.

**Claim 6** claims the processor-based system of claim 5 wherein said codec further includes a pair of analog-to-digital converters coupled to another one of said stereo channel pairs, one of said mixers also coupled to said pair of analog-to digital converts. As stated above apropos of claim 5, Intel meets all elements of that claim. Intel further discloses a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer, which read on "a pair of analog to digital converters coupled to another one of said stereo channel pairs, one of said mixers also couple to said pair of analog to digital converters". It would have been obvious to one of ordinary skill in the art to have a pair of A/D converters as claimed for the benefit of converting analog data to digital data.

**Claim 8** claims the processor-based system of claim 5 wherein said system can process two separate audio programs at the same time. As stated above apropos of claim 5, Intel meets all elements of that claim. Intel further teaches on page of 23 of an analog signal list comprising a microphone inputs and two CD audio inputs (CD\_L, and CD\_R) and two video audio inputs (Video\_1 and Video\_R). The CD audio and the video audio read on two separate audio programs. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to process two audio programs at the same time for the benefit of increasing the capability of the system. .

**Claim 10** claims the processor-based system of claim 5 wherein said digital interface includes a plurality of programmable ports so that the connections from the digital interface to said digital-to-analog converters might be changed. As stated above apropos of claim 1, Intel meets all elements of that claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to ensure that the digital interface would have a plurality of programmable ports for the benefit of being able to process different types of audio sources.

**Claim 11** claims the codec of claim 5 wherein said digital interface has a programmably changeable output data rate. As stated above apropos of claim 5, Intel's Audio Codec '97 meets all elements of that claim. Intel discloses on page 14 , paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. It would have been obvious to one of ordinary skill in the art to modify Intel's codec so that the digital interface can have a changeable output data rate for the benefit of mixing data.

4. Regarding **claim 12**, Intel's document, Audio Codec '97, explaining the features, operation etc. of the Audio Codec, comprises a block diagram of the functional blocks that make up the Audio Codec '97 (Figure 1) comprising a pair of D/A converters (DACs) which support a stereo PCM out channel; a digital interface; a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer; and an analog mixer. Intel further teaches on page of 23 of an analog signal list comprising a microphone inputs and two CD audio inputs (CD\_L, and CD\_R) and two video audio inputs (Video\_L and Video\_R). The CD audio and the video audio read on two separate audio programs. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo channel pair. Although Intel does not teach of a second pair of D/A converters coupled to another one of said stereo channel pairs, and another mixer to output the other audio program it would have been obvious under duplication of parts, *In Re Harza*, 274 F. 2d 669, 124, USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing a second audio program separately. . The claimed method is obviously present for one audio program and with the duplication of parts, would be present for two audio programs for the benefit of processing two audio programs separately.

**Claim 13** claims the method of claim 12 including receiving a third audio program in a Sony/Phillips digital interconnect format, formatting said third audio program and outputting said third audio program. As stated above apropos of claim 12, Intel meets all elements of that

claim. It is simply a design choice to receive a third audio program, to format it and output it as done with the two digital audio programs. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the program in a Sony/Phillips digital interconnect format for the benefit of transmit the data to another device.

**Claim 14** claims the method of claim 12 including outputting each of said audio programs through a different codec port and programmably changing the assignment of said programs to said ports. As stated above apropos of claim 12, Intel meets all elements of that claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to output each the audio programs through a different codec port, programmably changing the assignment of the ports for the benefit of being able to process different types of audio sources.

**Claim 15** claims the method of claim 12 including programmably changing the data rate of at least one of the said audio programs. As stated above apropos of claim 12, Intel meets all elements of that claim. Intel discloses on page 14, paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. It would have been obvious to one of ordinary skill in the art to modify Intel's method to include programmably changing the data rate of at least one of the audio for the benefit of being able to mix data.

**Claim 16** claims the method of claim 12 including mixing one of said audio programs in analog format with another analog signal.

5. Regarding **claim 17**, Intel's document, Audio Codec '97, explaining the features, operation etc. of the Audio Codec '97, comprises a block diagram of the functional blocks that

make up the Audio Codec '97 (Figure 1) comprising a pair of D/A converters (DACs) which support a stereo PCM out channel; a digital interface; a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer"; an analog mixer. The codec itself reads on "the article". It is obvious that some sort of medium is present in order for the codec to function properly. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo channel pair. D/A converters convert digital data to analog data. Intel discloses on page 14, paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. Although Intel does not teach of a second pair of D/A converters coupled to another one of said stereo channel pairs, and another mixer to output the other audio program it would have been obvious under duplication of parts, *In Re Harza*, 274 F. 2d 669, 124, USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing a second stereo channel separately. This reads on "programmably changing the assignment of said programs" as claimed. It is obvious to output the programs to different ports if they are being processed at the same time. This also reads on "receiving at least two digital programs" and "converting each of the digital audio programs" as claimed. It would have been obvious to one of ordinary skill in the art to modify Intel's codec so that the digital interface can have a changeable output data rate for the benefit of mixing data.

**Claim 18** claims the article of claim 17 further storing instructions that enable the processor- based system to programmably change the data rate of at least one of said audio programs. As stated above apropos of claim 17, Intel meets all elements of that claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to have instructions enabling the codec to output each the audio programs through a different codec port, programmably changing the assignment of the ports for the benefit of being able to process different types of audio sources.

6. Regarding **claim 20**, Intel's document, Audio Codec '97, explaining the features, operation etc. of the Audio Codec '97, comprises a block diagram of the functional blocks that make up the Audio Codec '97 (Figure 1) comprising a pair of D/A converters (DACs) which support a stereo PCM out channel; a digital interface; a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer"; an analog mixer. The codec itself reads on "the article". It is obvious that some sort of medium is present in order for the codec to function properly. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo channel pair. D/A converters convert digital data to analog data. Intel discloses on page 14, paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. This reads on "programmably changing the data rate" as claimed. Although Intel does not teach

of a second pair of D/A converters coupled to another one of said stereo channel pairs, and another mixer to output the other audio program it would have been obvious under duplication of parts, *In Re Harza*, 274 F. 2d 669, 124, USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing a second stereo channel separately. This reads on “receiving at least two digital programs” and “converting each of the digital audio programs” as claimed. It would have been obvious to one of ordinary skill in the art to modify Intel’s codec so that the digital interface can have a changeable output data rate for the benefit of mixing data.

**Claim 21** claims the article of claim 20 further storing instructions that enable the processor- based system to output each of said audio programs through a different codec port and programmably changing the assignment of said programs to said ports. As stated above apropos of claim 20, Intel meets all elements of that claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to have instructions enabling the codec to output each the audio programs through a different codec port, programmably changing the assignment of the ports for the benefit of being able to process different types of audio sources.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 7,19, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel's Audio Codec in view of Mayo (U.S. Patent 5,133,081).

**Claim 7** claims the processor-based system of claim 6 wherein said system may simultaneously play one audio program while recording another audio program. As stated above apropos of claim 6, Intel meets all elements of that claim. Intel teaches that the Audio Codec '97 has recording capability. Mayo teaches of a system comprising two codecs capable of simultaneously recording and playing messages using the same recording medium (column 10, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Intel's audio codec by incorporating another codec for the benefit of not having any interference between the two functions.

**Claim 19** claims the article of claim 17 further storing instructions that enable the processor-based system to play one audio program while recording another audio program. As stated above apropos of claim 17, Intel meets all elements of that claim. Mayo teaches of a system comprising two codecs capable of simultaneously recording and playing messages using the same recording medium (column 10, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Intel's audio codec by incorporating another codec for the benefit of not having any interference between the two functions.

**Claim 22** claims the article of claim 20 further storing instructions that enable the processor-based system to play one audio program while recording another audio program. As stated above apropos of claim 20, Intel meets all elements of that claim. Mayo teaches of a system comprising two codecs capable of simultaneously recording and playing messages using

the same recording medium (column 10, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Intel's audio codec by incorporating another codec for the benefit of not having any interference between the two functions.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 703-305-4359. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

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PRIMARY EXAMINER